RDA7088

SINGLE-CHIP BROADCAST FM RADIO TUNER

Rev.1.1–Jun.2009

General Description

The RDA7088 is a single-chip broadcast FM stereo radio tuner with fully integrated synthesizer, IF selectivity and MPX decoder. The tuner uses the CMOS process, require the least external component. The package size is SOP16 and is completely adjustment-free. All these make it very suitable for portable devices.

The RDA7088 has a powerful low-IF digital audio processor, this make it have optimum sound quality with varying reception conditions.

The RDA7088 can be tuned to the worldwide frequency band.

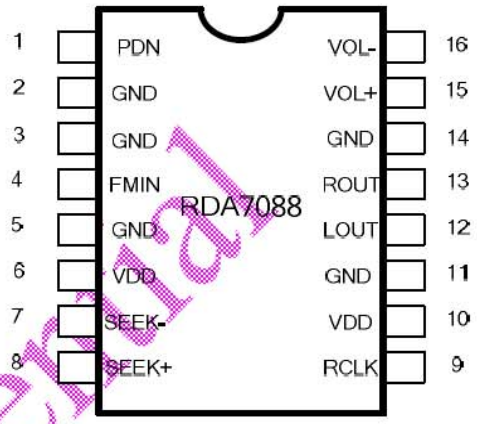


Figure 1-1. RDA7088 Top View

1.1 Features

- CMOS single-chip fully-integrated FM tuner
- Low power consumption
  - Total current consumption lower than 17mA at 3.0V power supply
- Support worldwide frequency band
  - 76-108 MHz
- Default Frequency
  - 107.9MHz
- Fulll band seek time
  - < 5s
- Autonomous search tuning
- Support 32.768KHz crystal oscillator
- Digital auto gain control (AGC)
- Volume control
- Line-level analog output voltage
- Directly support 32Ω resistance loading
- Integrated LDO regulator
  - 1.8 to 3.6 V operation voltage
- SOP16 pin package

1.2 Applications

- Cellular handsets
- MP3, MP4 players
- Portable radios
- PDAs, Notebook

2 Receiver Characteristics

VDD = 1.8 to 3.6 V, T_A = -25 to 85 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications						
F_{in}	FM Input Frequency		76		108	MHz
V_{rf}	Sensitivity[1,2,3]	(S+N)/N=26dB		1.6	2	μV EMF
α_{am}	AM Suppression[1,2]	m=0.3	40	-	-	dB
V_{AFL}; V_{AFR}	Left and Right Audio Frequency Output Voltage (Pins LOUT and ROUT)				200	mV
(S+N)/N	Maximum Signal Plus Noise to Noise Ratio[1,2,3,5]		58	60	-	dB
α_{SCS}	Stereo Channel Separation		35	-	-	dB
THD	Audio Total Harmonic Distortion[1,3,6]			0.05	0.1	%
R_L	Audio Output Loading Resistance	Single-ended	32	-	-	Ω
$I_{power\ up}$			-	-	20	mA
$I_{power\ down}$			-	-	10	μA

3 Pins Description

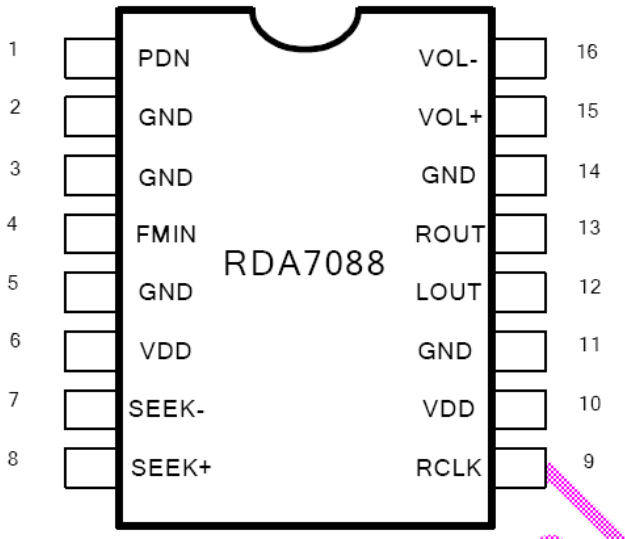


Figure 3-1. RDA7088 Top View

Table 3-1 RDA7088 Pins Description

SYMBOL	PIN	DESCRIPTION
GND	2,3,5,11,14	Ground. Connect to ground plane on PCB
FM_IN	4	FM single input
RCLK	9	32.768KHz reference clock input
VDD	6,10	Power supply
LOUT,ROUT	12,13	Right/Left audio output
SEEK-,SEEK+	7,8	seek up,seek down
VOL+,VOL-	15,16	Volume control
PN	1	Powerup/powerdown Enable

4 Application Diagram

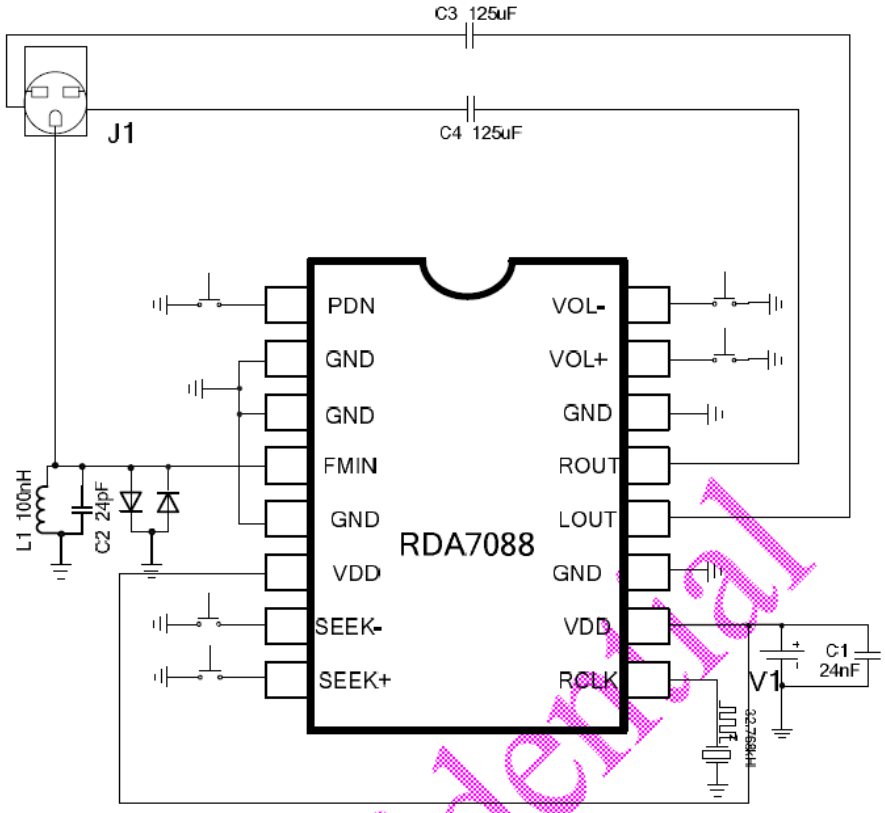


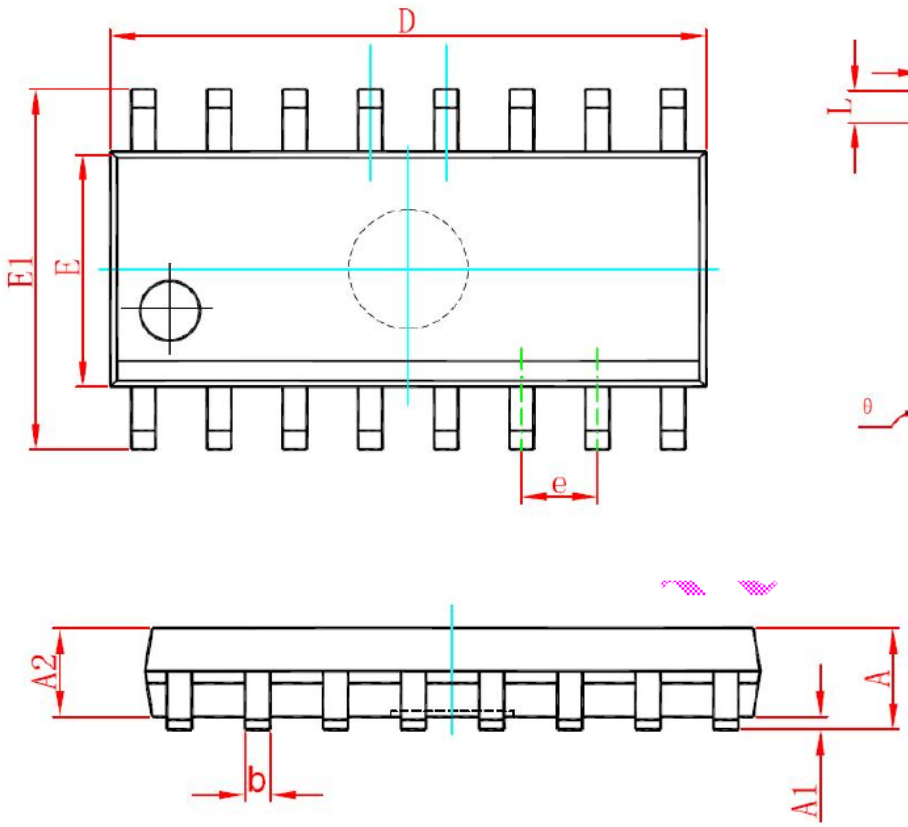
Figure 4-2. RDA7088 FM Tuner Application Diagram

Table 4-3 Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA7088	Broadcast FM Radio Tuner	RDA
J1		Common 32Ω Resistance Headphone	
L1/C2	100nH/24pF	LC Chock for LNA Input	Murata
C4,C5	125μF	Audio AC Couple Capacitors	Murata
C1	24nF	Power Supply Bypass Capacitor	Murata

5 Package Physical Dimension

Figure 5-1 illustrates the package details for the RDA7088. The package is lead-free and RoHS-compliant.



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
Θ	1°	7°	1°	7°
L	0.400	1.270	0.016	0.050

Figure 5-1. 16 PIN SOP

PCB Land Pattern

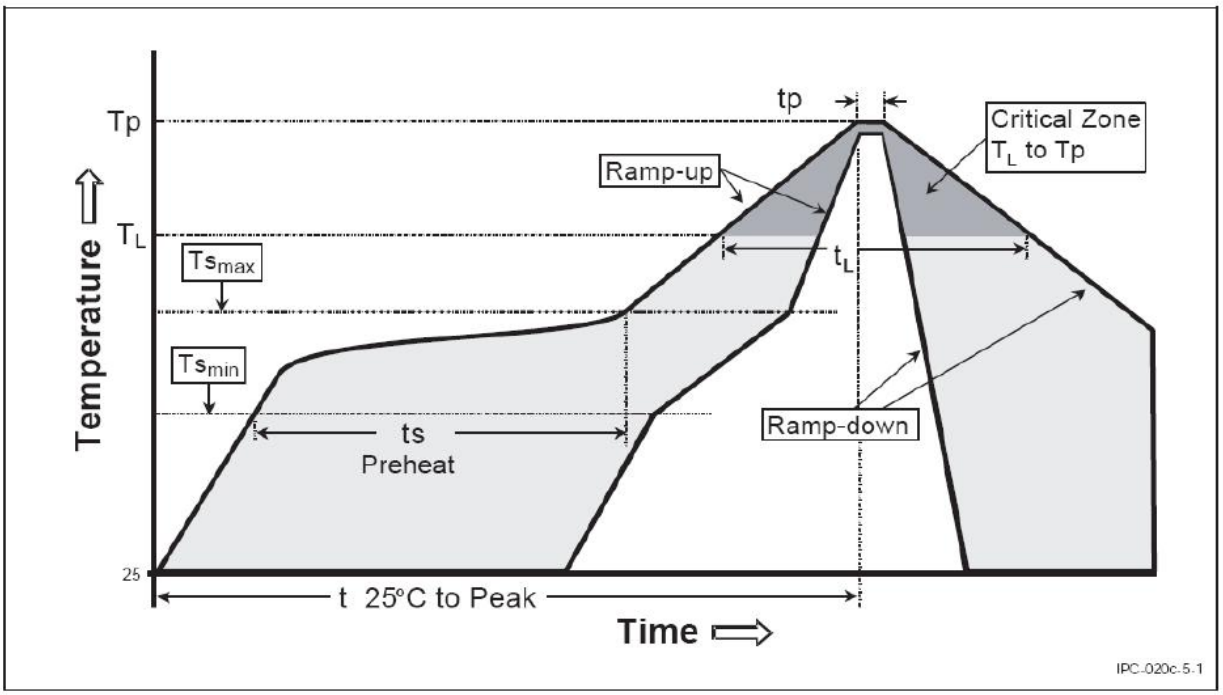


Figure 5-4.Classification Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (T_{Smax} to T_p)	3 °C/second max.	3 °C/second max.
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (t_{smin} to t_{smax})	 100 °C 100 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: -Temperature (T_L) -Time (t_L)	 183 °C 60-150seconds	 217°C 60-150 seconds
Peak /Classification Temperature(T_p)	See Table-II	See Table-III
Time within 5 °C of actual Peak Temperature (t_p)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Table-I Classification Reflow Profiles

Package Thickness	Volume mm^3 <350	Volume mm^3 ⩾350
<2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
⩾2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

Table – II SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm – 2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
⩾2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *
*Tolerance : The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level.			

Table – III Pb-free Process – Package Classification Reflow Temperatures

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 °C, - X °C (based on machine variation capability)whatever

is required to control the profile process but at no time will it exceed - 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table –III.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

Note 5: Components intended for use in a "lead-free" assembly process **shall** be evaluated using the "lead free" classification temperatures and profiles defined in Table-I II III whether or not lead free.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

Change List

REV	DATE	AUTHER	CHANGE DESCRIPTION
V1.0	2009-05-26	ChunZhao,YananLiu,XiaoqiYou	Original Draft.
V1.1	2009-06-03	ChunZhao,YananLiu,XiaoqiYou	Change Package to SOP16